REMARKS/ARGUMENTS

Favorable reconsideration of this application as currently amended and in light of the following discussion is respectfully requested.

Claims 1-36 are pending in the present application. Claims 1, 13, 25-27, and 29 are amended by the present amendment.

In the outstanding Office Action, Claims 30-36 have been withdrawn from consideration; Claims 13-24 were objected to; Claim 29 was rejected under 35 U.S.C. § 112, second paragraph; Claim 29 was rejected under 35 U.S.C. § 103(a) as unpatentable over Dennison et al. (U.S. Patent No. 6,537,891 B1, herein "Dennison"); and Claims 1-12 and 25-28 were indicated as allowable.

Applicants thanks the Examiner for the indication of allowable subject matter.

Claims 1, 13, and 25-27 have been amended to clarify that a "memory cell transistor" is part of "a memory cell" without adding new matter.

Regarding the objection to Claims 13-24, Claim 13 has been amended to recite "the semiconductor layer" instead of the "first semiconductor layer" as suggested in the outstanding Office Action. No new matter has been added. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the rejection of Claim 29 under 35 U.S.C. § 112, second paragraph, Claim 29 has been amended to more clearly recite a first gate electrode and a first gate insulating film provided on a first surface, a second surface, and a third surface of a first semiconductor layer. The claim amendments find support in Figures 25 and 26 and their corresponding description in the specification. No new matter has been added. Accordingly, it is respectfully requested this rejection be withdrawn.

Regarding the rejection of Claim 29 under 35 U.S.C. § 103(a) as unpatentable over Dennison, independent Claim 29 has been amended to recite:

a first semiconductor layer provided on the insulating film and having a first surface, a second surface opposite to the first surface and a third surface contacting the first surface and the second surface;

a first memory cell transistor constituting a part of a memory cell in an SRAM[[,]] and having a first gate electrode and first source/drain diffusion layers, the first gate electrode being provided on a gate insulating film which is provided on the first surface, on the second surface and on the third surface of the first semiconductor layer, the first source/drain diffusion layers sandwiching a region enclosed by the first gate electrode in the first semiconductor layer.

The claim amendments find support in the specification at page 34, lines 1-12, and in Figure 26. No new matter has been added.

As shown in Figure 26, the claimed semiconductor device includes a first semiconductor layer 13a having a first surface (left hand surface), a second surface (right hand surface) opposite to the first surface, and a third surface (top surface) contacting the first surface and the second surface. A gate electrode 24 is provided on a gate insulating film 23 on the first surface, the second surface, and the third surface of the first semiconductor layer 13a.

The semiconductor device of Claim 29 advantageously reduces variations in a threshold voltage of a cell transistor and an occurrence of errors by depleting the first semiconductor layer, except the source/drain layers, and by using a partially-depleted type peripheral transistor.[1] In addition, the claimed device advantageously provides a desired threshold voltage for the peripheral transistor.

Turning to the applied art, Dennison shows in Figure 6 a peripheral gate oxide layer 86 provided on an upper silicon layer 14 on a BOX layer 12, and a peripheral transistor gate 82 provided on the peripheral gate oxide layer 86. However, Dennison does not teach or suggest the gate electrode being provided on a gate insulting film provided on a first surface, a second surface, and a third surface of a first semiconductor layer.

[1] See specification, page 34, lines 14-22, and page 24, line 18, to page 25, line 6.

On the contrary, Dennison shows in Figure 6 that both the chip periphery transistor and the chip memory array transistor have the gate electrodes 82 and 54 and the gate insulating films 86 and 52 provided only on one side (top surface) of the semiconductor layers 26 and 24, and not on the first surface, the second surface, and the third surface of the semiconductor layers 26 and 24 as required by independent Claim 29.

Accordingly, it is respectfully submitted that amended independent Claim 29 patentably distinguishes over Dennison.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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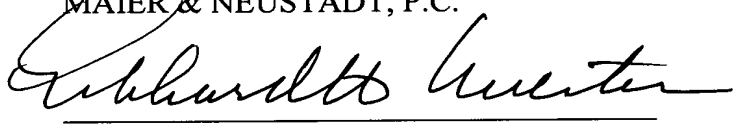

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